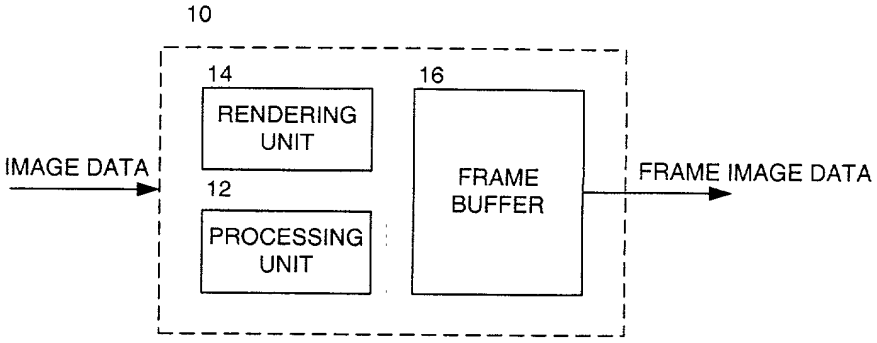

FIG. 1
(Prior Art)

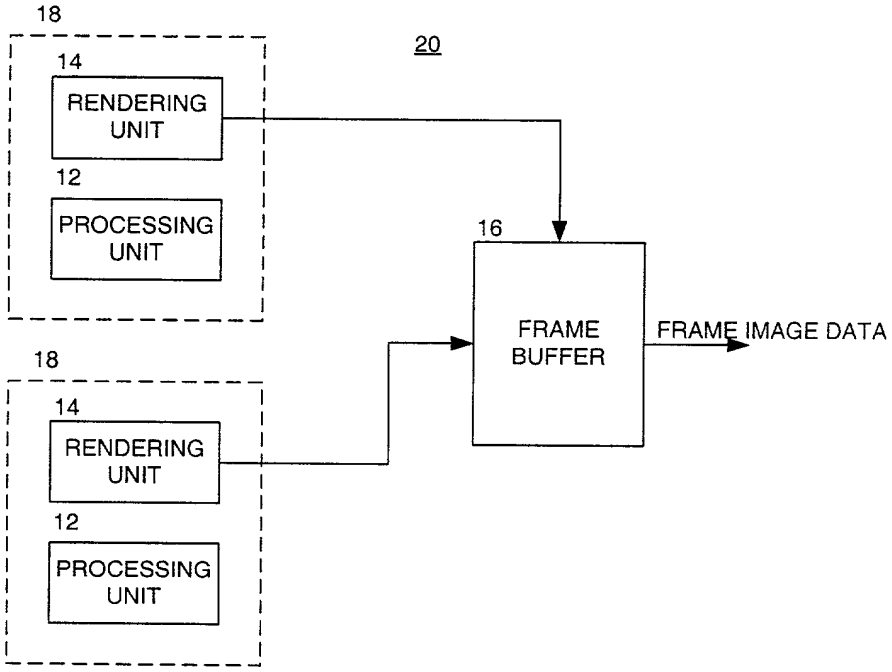

FIG. 2
(Prior Art)

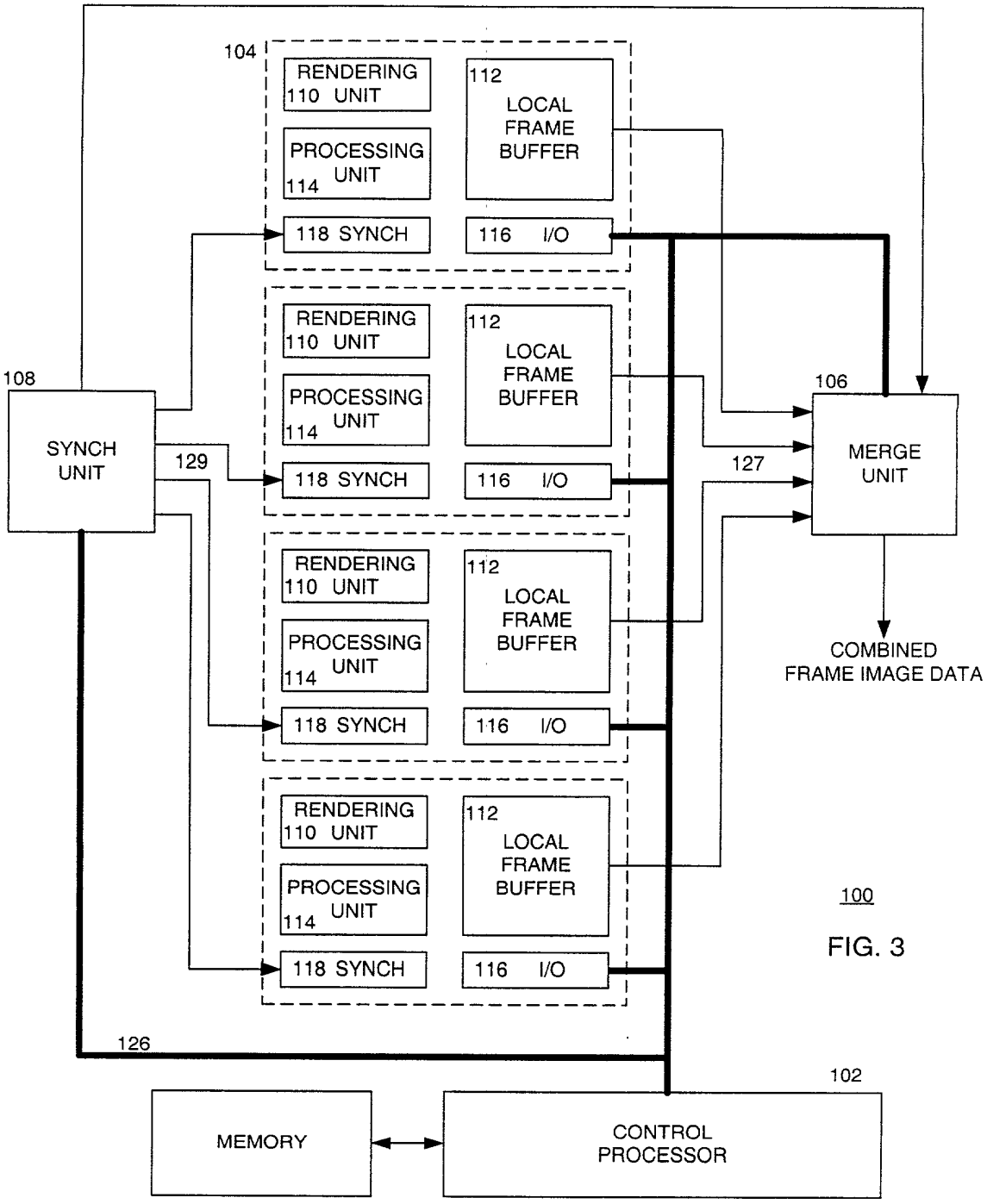
104
RENDERING 110 UNIT
PROCESSING 114 UNIT
112 LOCAL FRAME BUFFER
118 SYNCH
116 I/O
108
SYNCH UNIT
129
127
106
MERGE UNIT
COMBINED FRAME IMAGE DATA
100
126
102
MEMORY
CONTROL PROCESSOR

FIG. 3

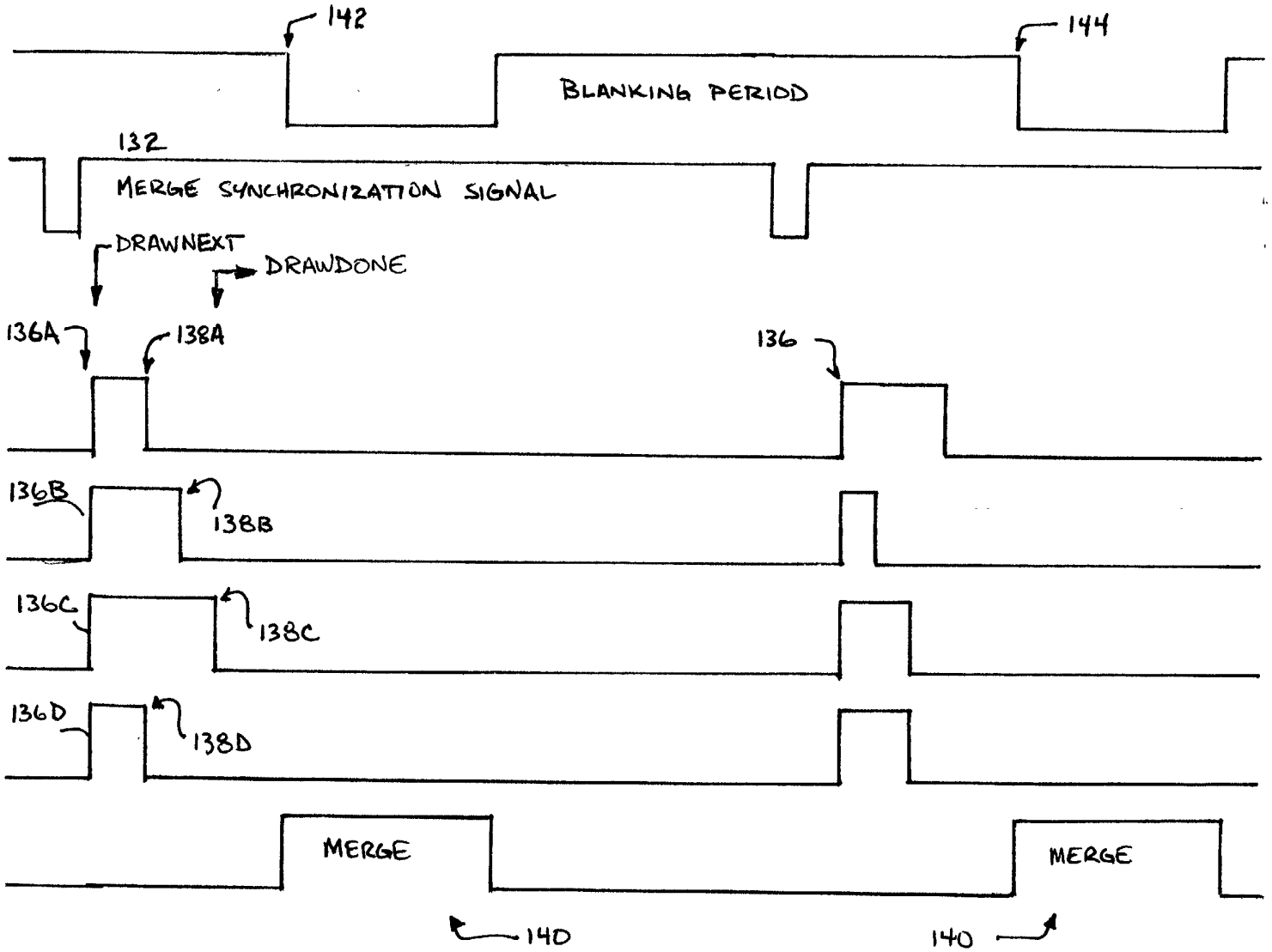

FIG. 4

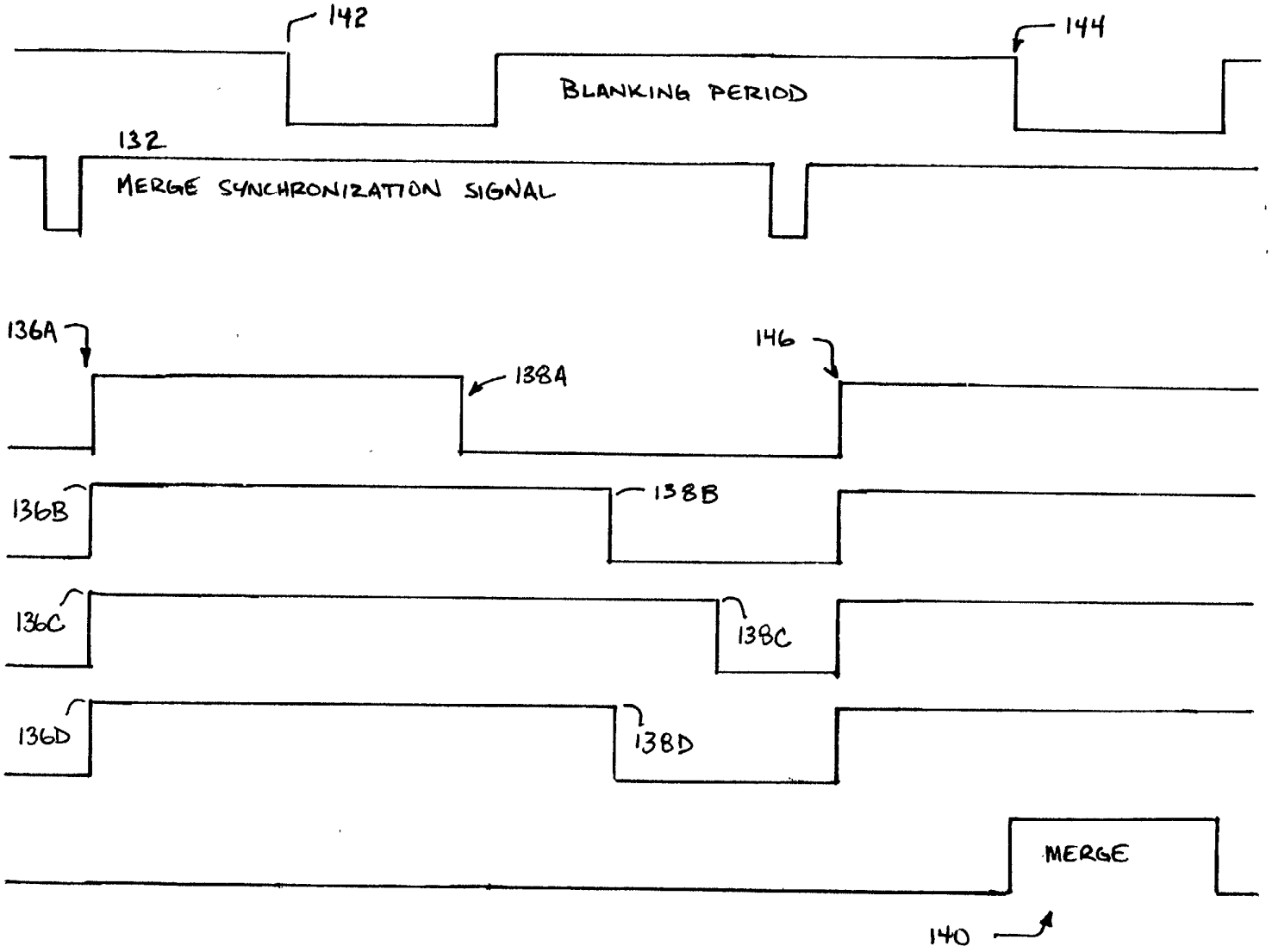
142
144
BLANKING PERIOD
132
MERGE SYNCHRONIZATION SIGNAL
136A
138A
146
136B
138B
136C
138C
136D
138D
MERGE
140

FIG. 5

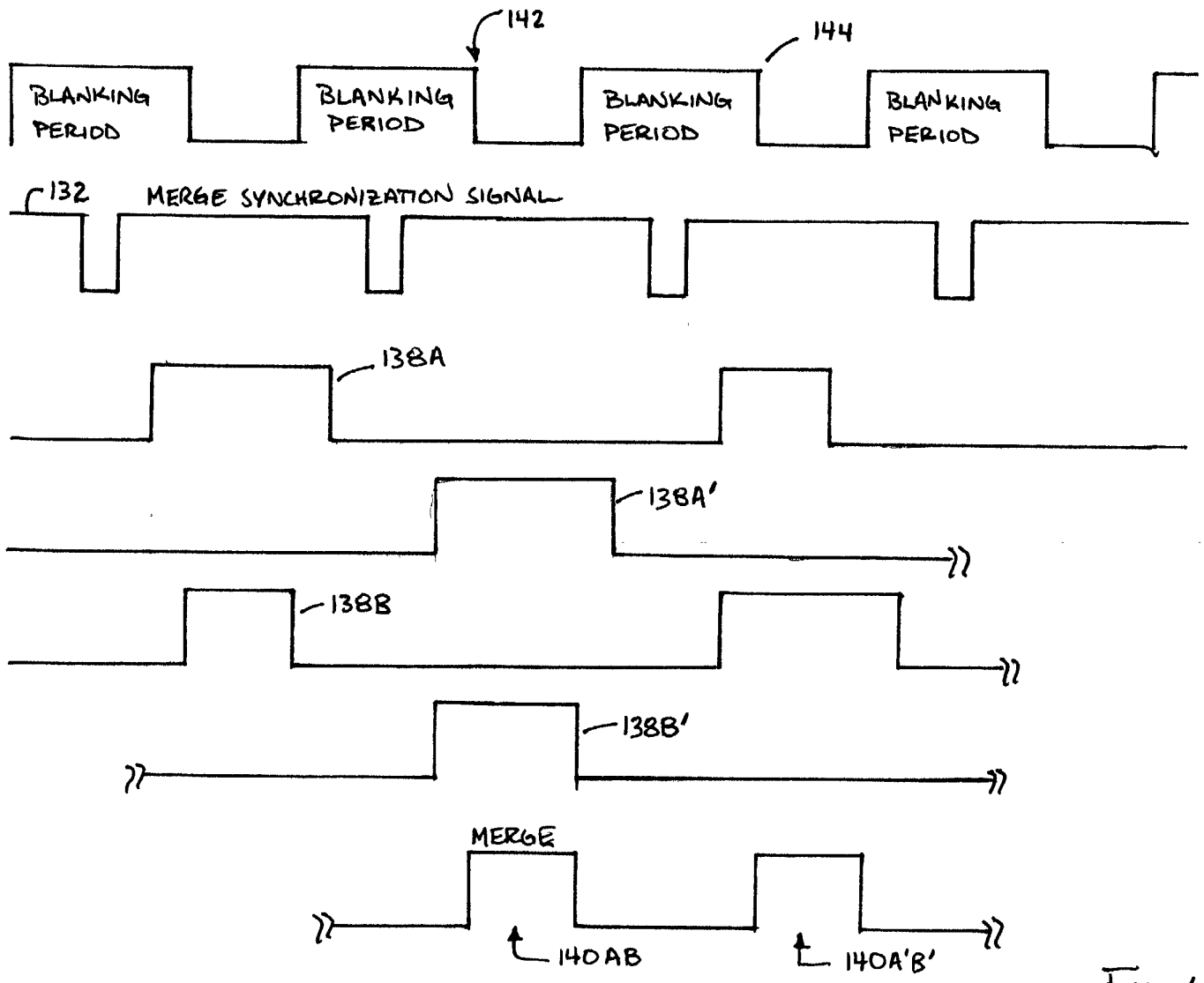
142
144
BLANKING PERIOD
BLANKING PERIOD
BLANKING PERIOD
BLANKING PERIOD
132
MERGE SYNCHRONIZATION SIGNAL
138A
138A'
138B
138B'
MERGE
140AB
140A'B'

FIG. 6A

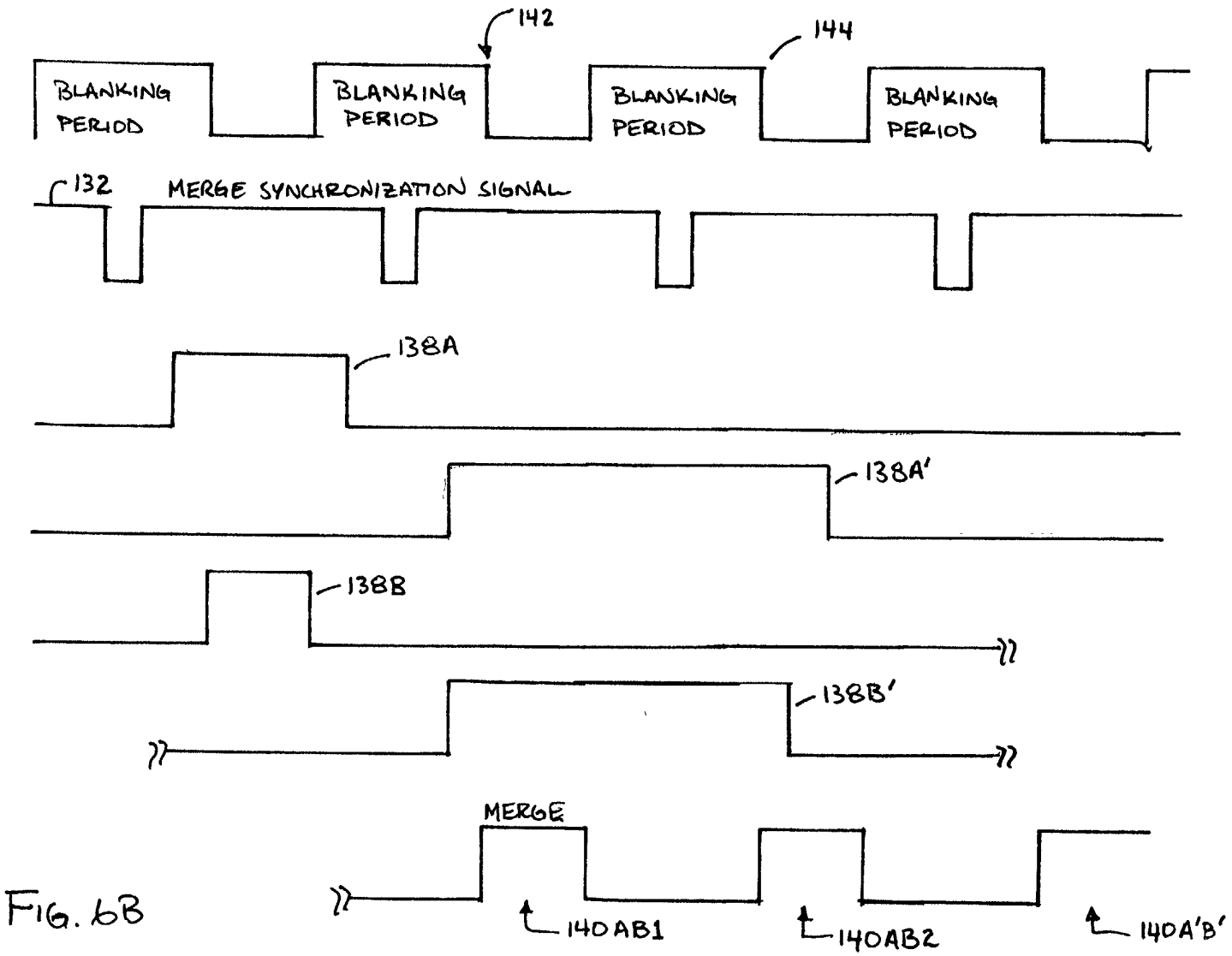

FIG. 6B

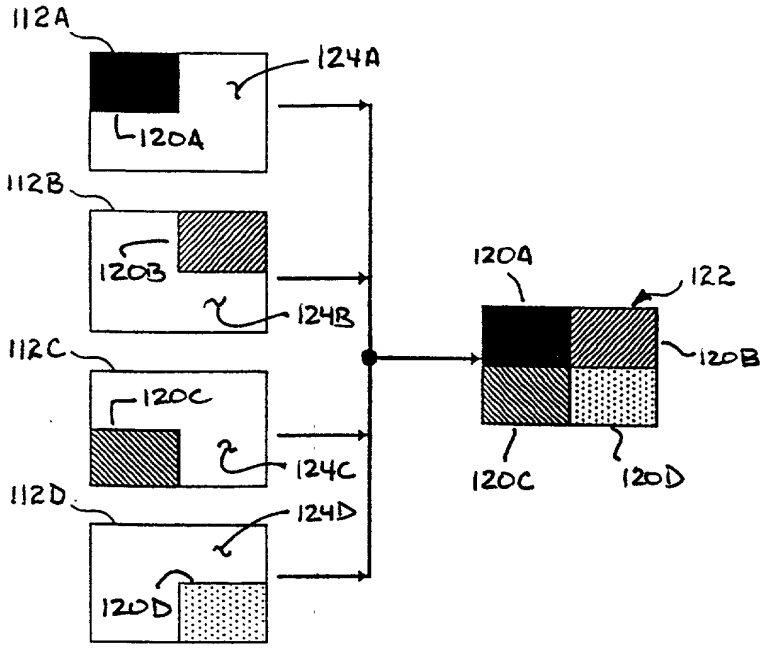
112A
124A
120A
112B
120B
124B
112C
120C
124C
112D
124D
120D
120A
122
120B
120C
120D

FIG. 7A

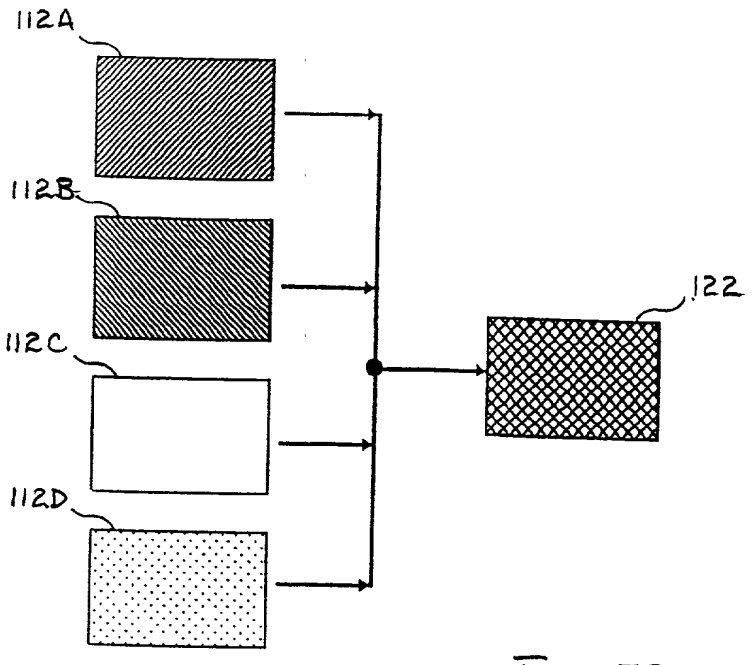

FIG. 7B

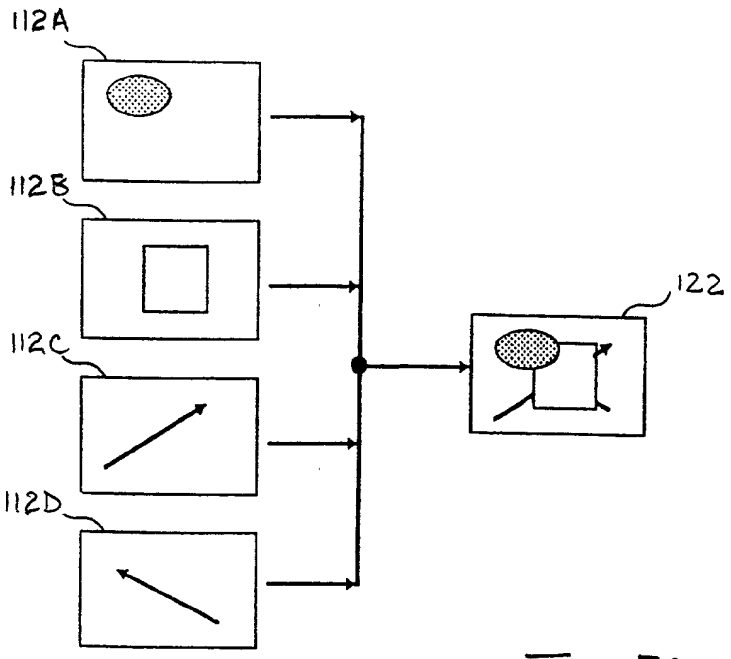

FIG. 7C

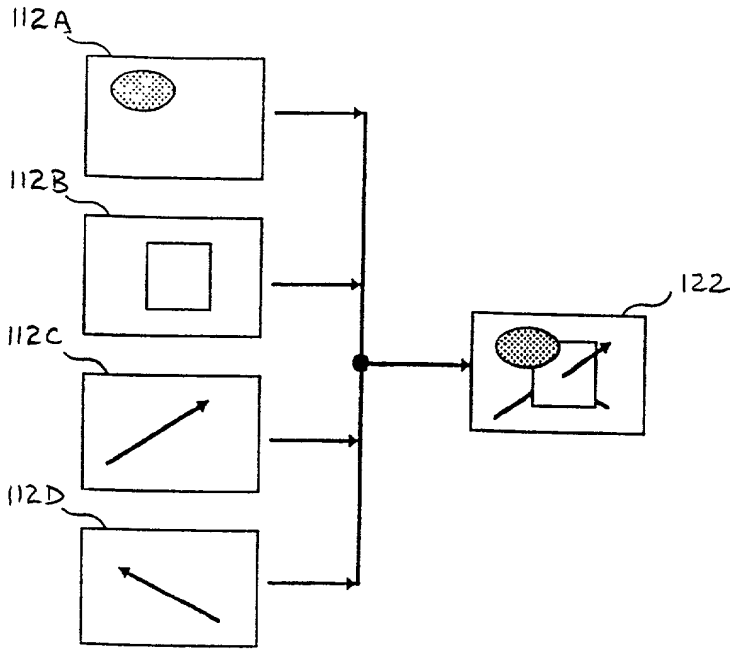

FIG. 7D

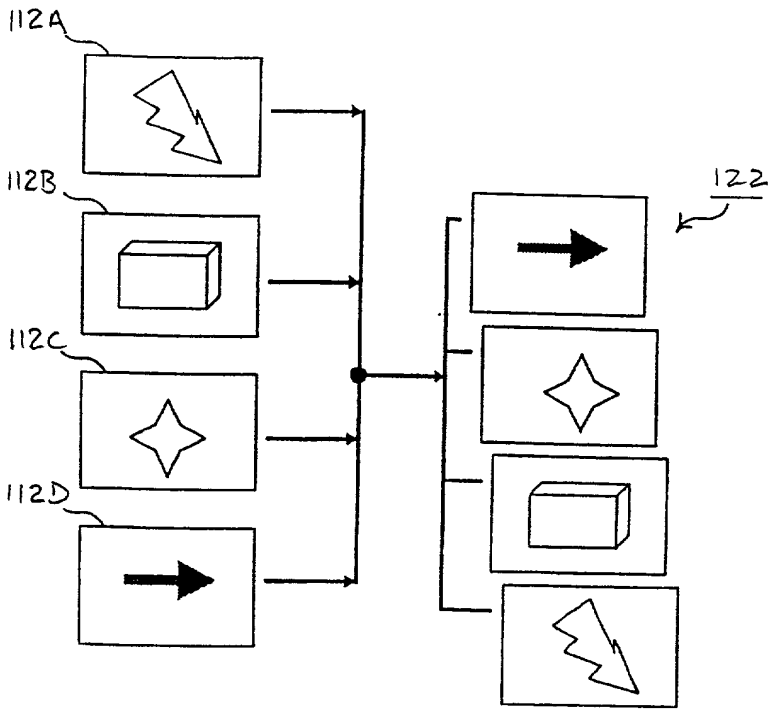

FIG. 7E

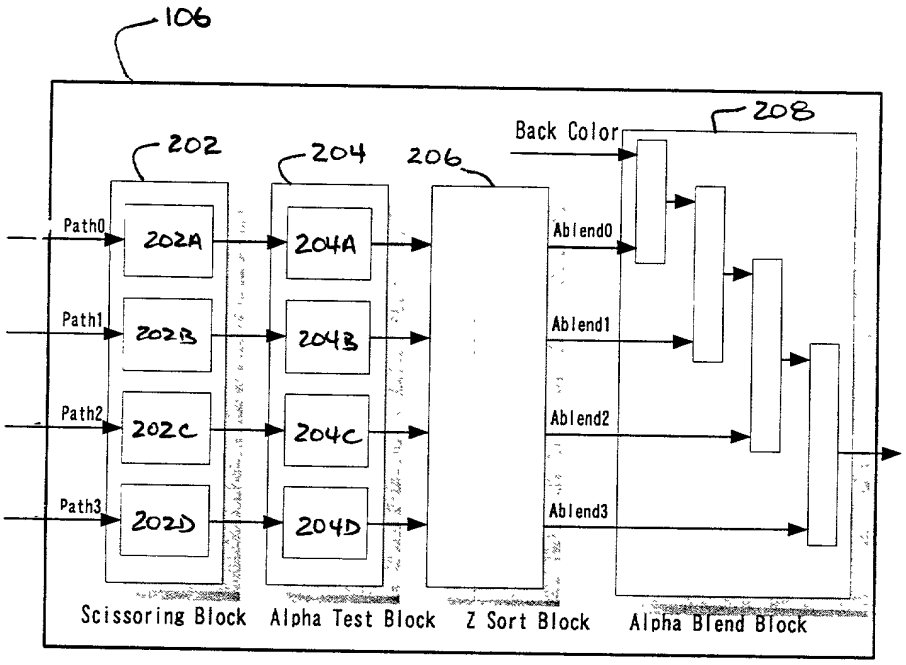
106
202
204
206
208
Back Color
Path0
Path1
Path2
Path3
202A
202B
202C
202D
204A
204B
204C
204D
Ablend0
Ablend1
Ablend2
Ablend3
Scissoring Block
Alpha Test Block
Z Sort Block
Alpha Blend Block

FIG. 8.

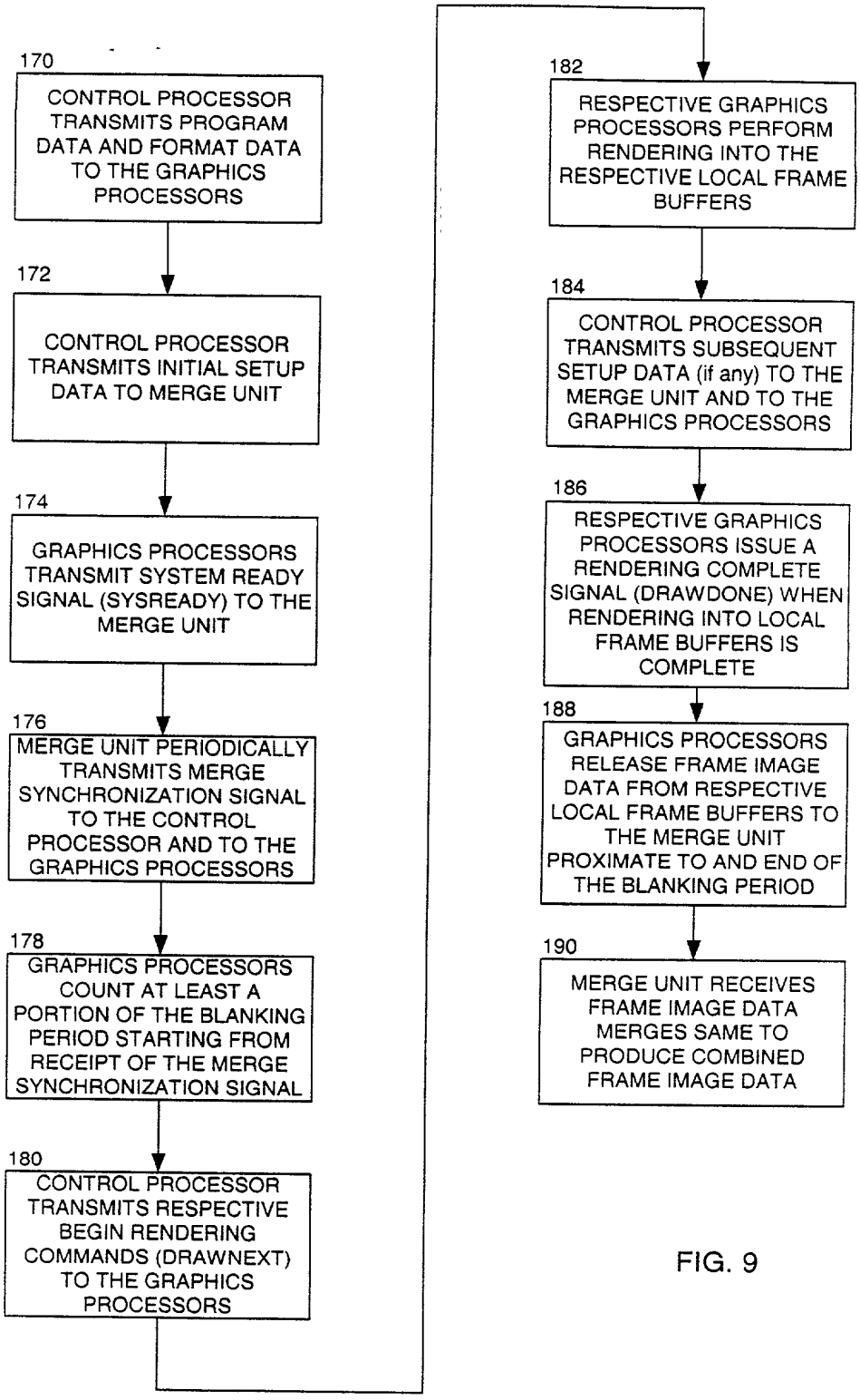
170
CONTROL PROCESSOR TRANSMITS PROGRAM DATA AND FORMAT DATA TO THE GRAPHICS PROCESSORS
172
CONTROL PROCESSOR TRANSMITS INITIAL SETUP DATA TO MERGE UNIT
174
GRAPHICS PROCESSORS TRANSMIT SYSTEM READY SIGNAL (SYSREADY) TO THE MERGE UNIT
176
MERGE UNIT PERIODICALLY TRANSMITS MERGE SYNCHRONIZATION SIGNAL TO THE CONTROL PROCESSOR AND TO THE GRAPHICS PROCESSORS
178
GRAPHICS PROCESSORS COUNT AT LEAST A PORTION OF THE BLANKING PERIOD STARTING FROM RECEIPT OF THE MERGE SYNCHRONIZATION SIGNAL
180
CONTROL PROCESSOR TRANSMITS RESPECTIVE BEGIN RENDERING COMMANDS (DRAWNEXT) TO THE GRAPHICS PROCESSORS
182
RESPECTIVE GRAPHICS PROCESSORS PERFORM RENDERING INTO THE RESPECTIVE LOCAL FRAME BUFFERS
184
CONTROL PROCESSOR TRANSMITS SUBSEQUENT SETUP DATA (if any) TO THE MERGE UNIT AND TO THE GRAPHICS PROCESSORS
186
RESPECTIVE GRAPHICS PROCESSORS ISSUE A RENDERING COMPLETE SIGNAL (DRAWDONE) WHEN RENDERING INTO LOCAL FRAME BUFFERS IS COMPLETE
188
GRAPHICS PROCESSORS RELEASE FRAME IMAGE DATA FROM RESPECTIVE LOCAL FRAME BUFFERS TO THE MERGE UNIT PROXIMATE TO AND END OF THE BLANKING PERIOD
190
MERGE UNIT RECEIVES FRAME IMAGE DATA MERGES SAME TO PRODUCE COMBINED FRAME IMAGE DATA

FIG. 9

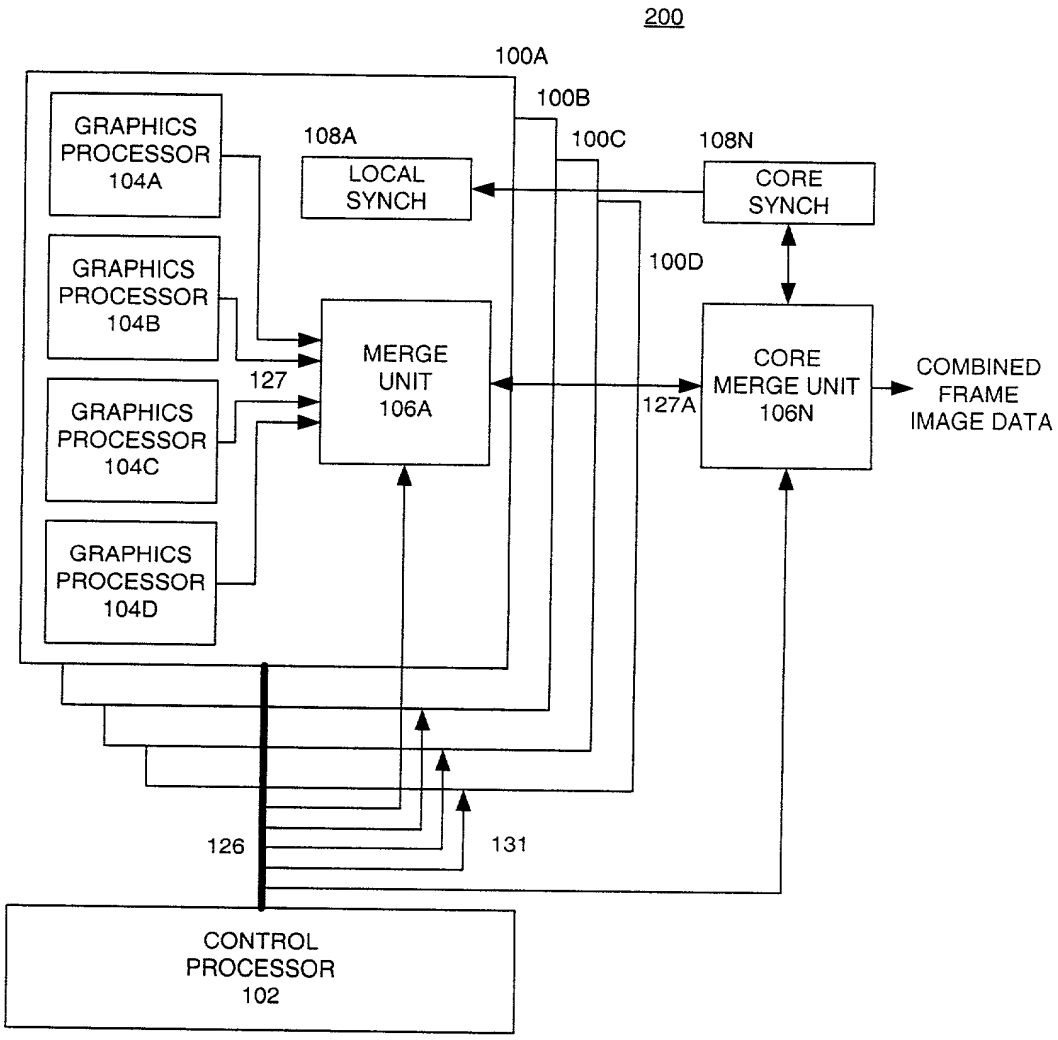
200
100A
100B
100C
100D
GRAPHICS PROCESSOR 104A
GRAPHICS PROCESSOR 104B
GRAPHICS PROCESSOR 104C
GRAPHICS PROCESSOR 104D
108A
LOCAL SYNCH
108N
CORE SYNCH
MERGE UNIT 106A
127
127A
CORE MERGE UNIT 106N
COMBINED FRAME IMAGE DATA
126
131
CONTROL PROCESSOR 102

FIG. 10

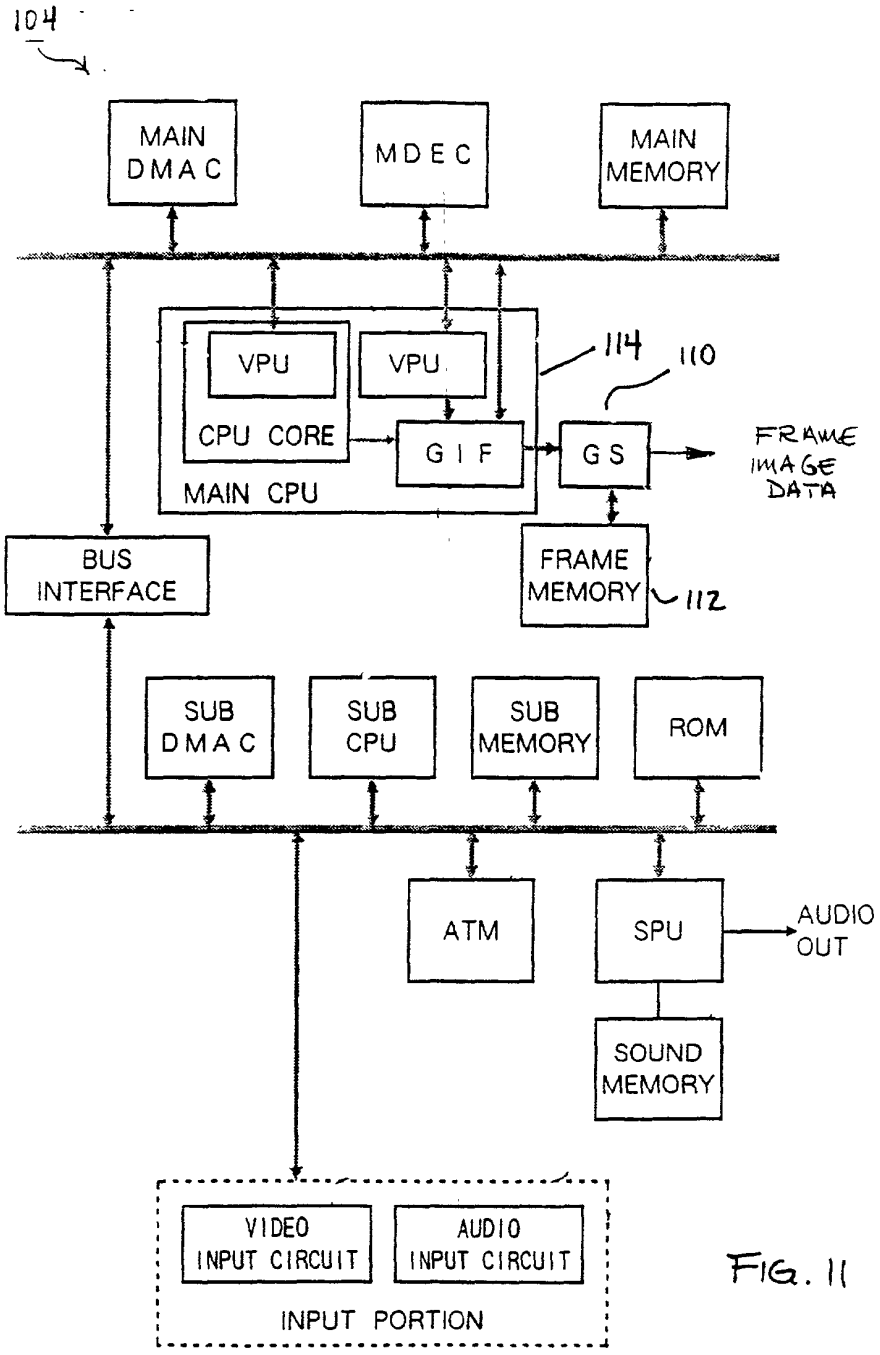
104
MAIN DMAC
MDEC
MAIN MEMORY
VPU
VPU
CPU CORE
GIF
GS
114
110
MAIN CPU
FRAME IMAGE DATA
BUS INTERFACE
FRAME MEMORY
112
SUB DMAC
SUB CPU
SUB MEMORY
ROM
ATM
SPU
AUDIO OUT
SOUND MEMORY
VIDEO INPUT CIRCUIT
AUDIO INPUT CIRCUIT
INPUT PORTION

FIG. 11

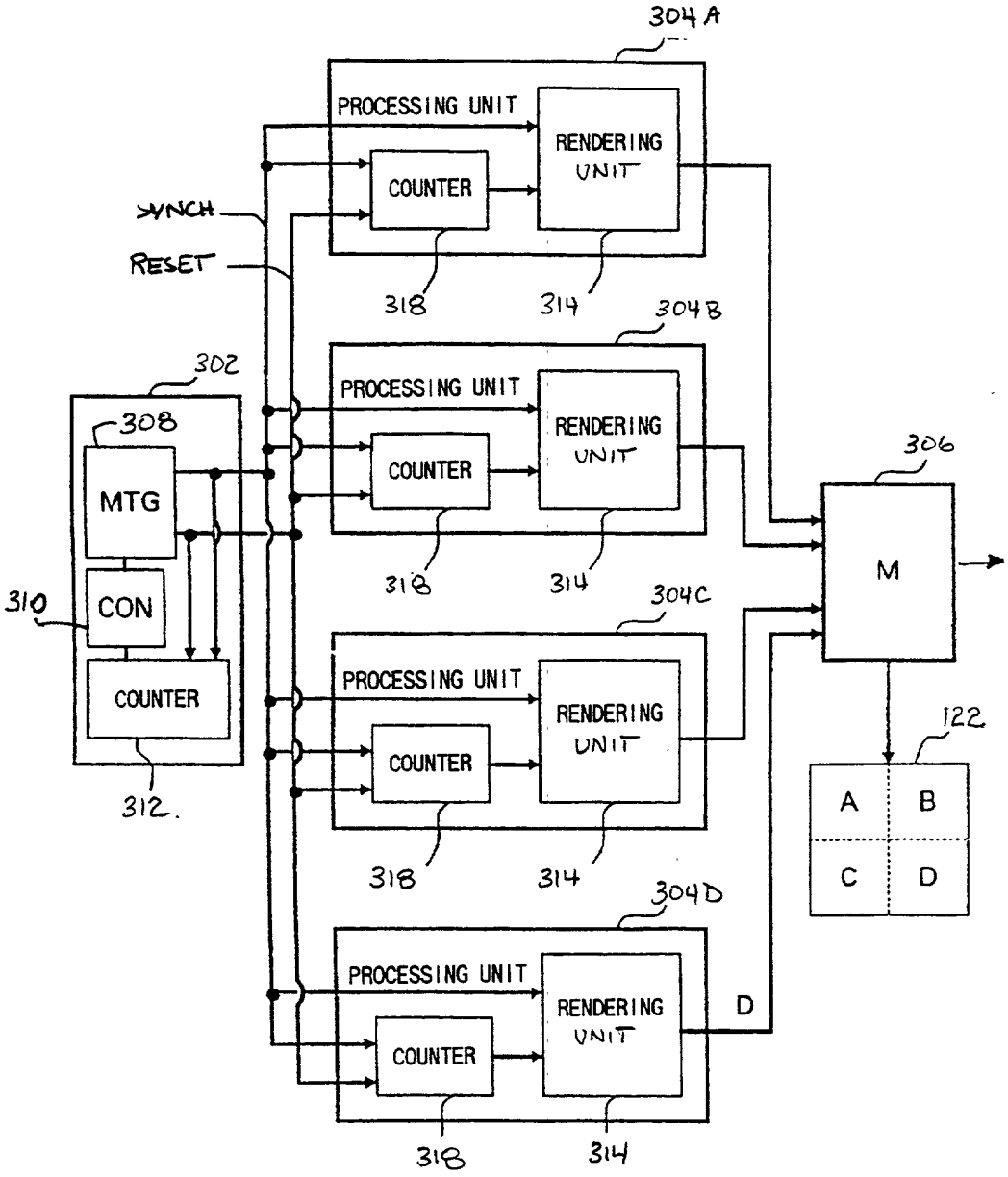
304A
PROCESSING UNIT
RENDERING UNIT
COUNTER
SYNCH
RESET
318
314
304B
302
308
MTG
CON
COUNTER
310
312
306
M
304C
122
A
B
C
D
304D
D

Fig. 12

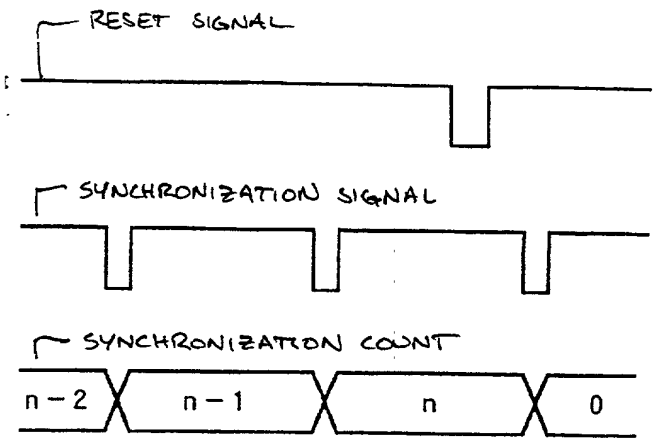

FIG. 13A

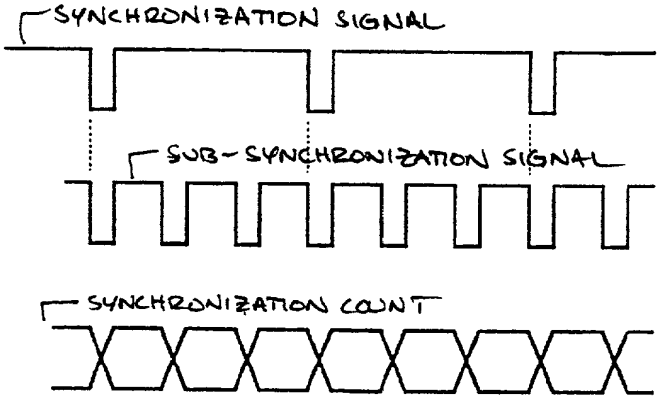

FIG. 13B

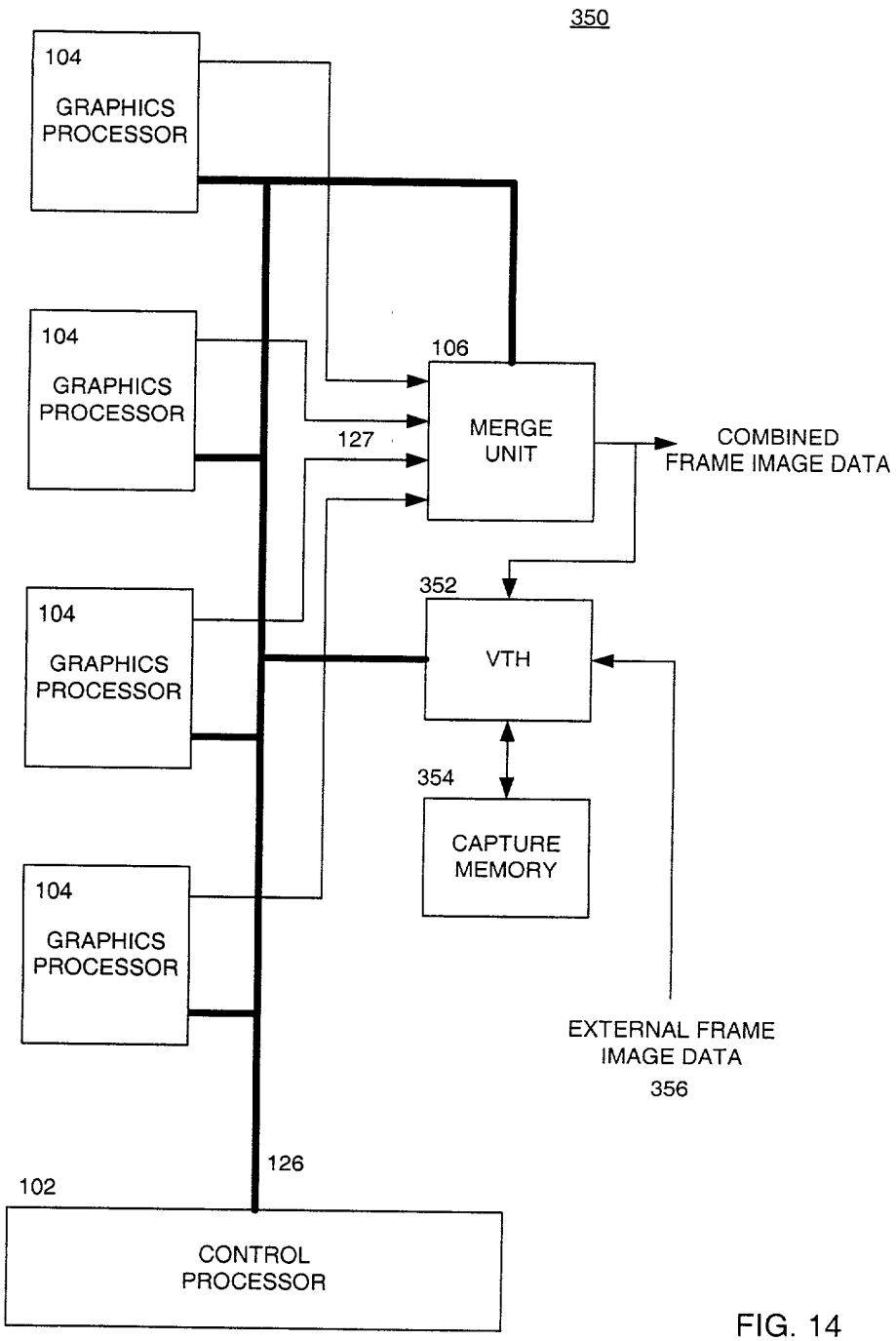
350
104
GRAPHICS PROCESSOR
104
GRAPHICS PROCESSOR
104
GRAPHICS PROCESSOR
104
GRAPHICS PROCESSOR
106
MERGE UNIT
127
COMBINED FRAME IMAGE DATA
352
VTH
354
CAPTURE MEMORY
EXTERNAL FRAME IMAGE DATA
356
126
102
CONTROL PROCESSOR

FIG. 14

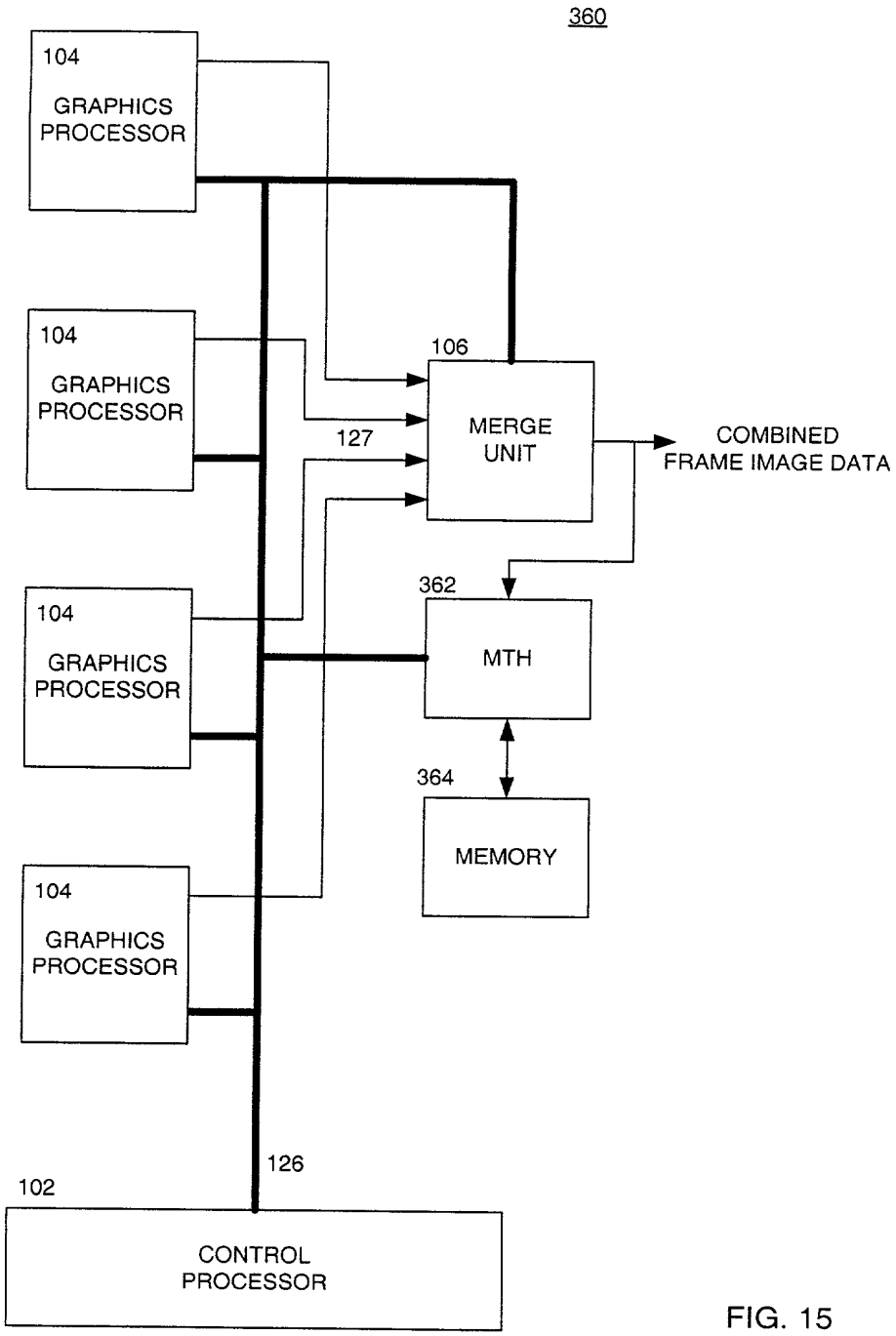
360
104
GRAPHICS PROCESSOR
104
GRAPHICS PROCESSOR
106
MERGE UNIT
127
COMBINED FRAME IMAGE DATA
362
104
GRAPHICS PROCESSOR
MTH
364
MEMORY
104
GRAPHICS PROCESSOR
126
102
CONTROL PROCESSOR

FIG. 15

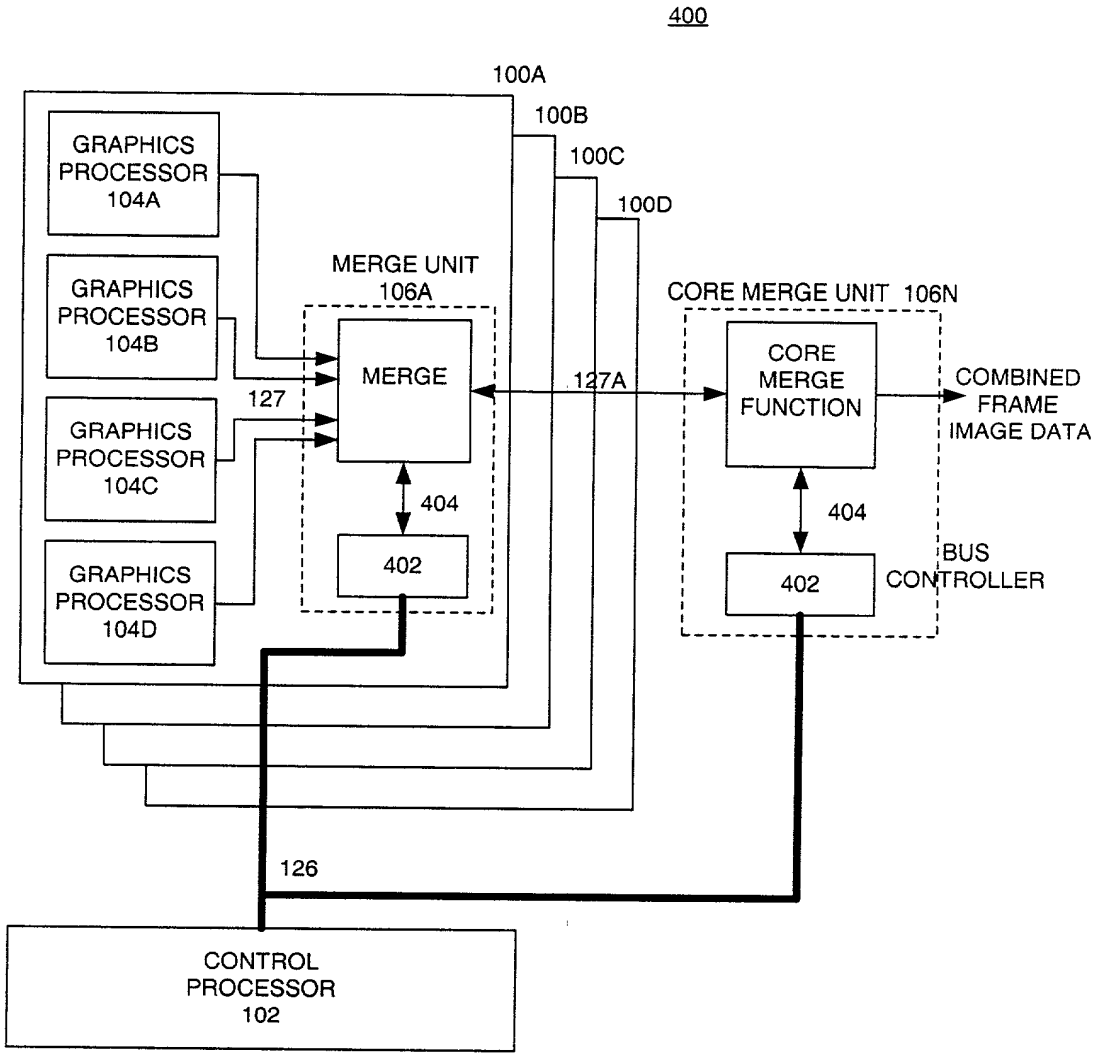
400
100A
100B
100C
100D
GRAPHICS PROCESSOR 104A
GRAPHICS PROCESSOR 104B
GRAPHICS PROCESSOR 104C
GRAPHICS PROCESSOR 104D
MERGE UNIT 106A
MERGE
127
404
402
127A
CORE MERGE UNIT 106N
CORE MERGE FUNCTION
COMBINED FRAME IMAGE DATA
404
402
BUS CONTROLLER
126
CONTROL PROCESSOR 102

FIG. 16

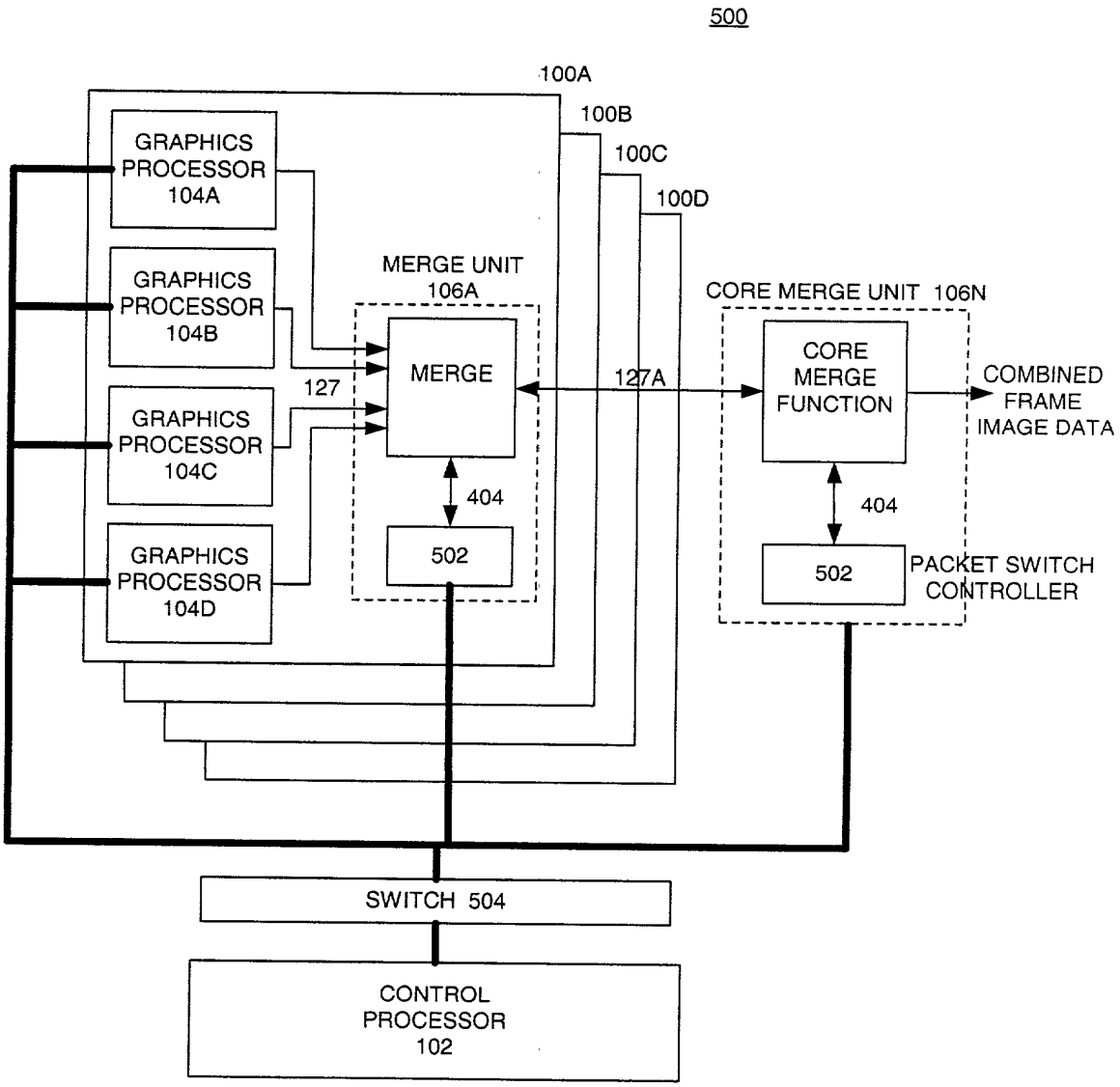
500
100A
100B
100C
100D
GRAPHICS PROCESSOR 104A
GRAPHICS PROCESSOR 104B
GRAPHICS PROCESSOR 104C
GRAPHICS PROCESSOR 104D
MERGE UNIT 106A
MERGE
127
127A
404
502
CORE MERGE UNIT 106N
CORE MERGE FUNCTION
COMBINED FRAME IMAGE DATA
404
502
PACKET SWITCH CONTROLLER
SWITCH 504
CONTROL PROCESSOR 102

FIG. 17

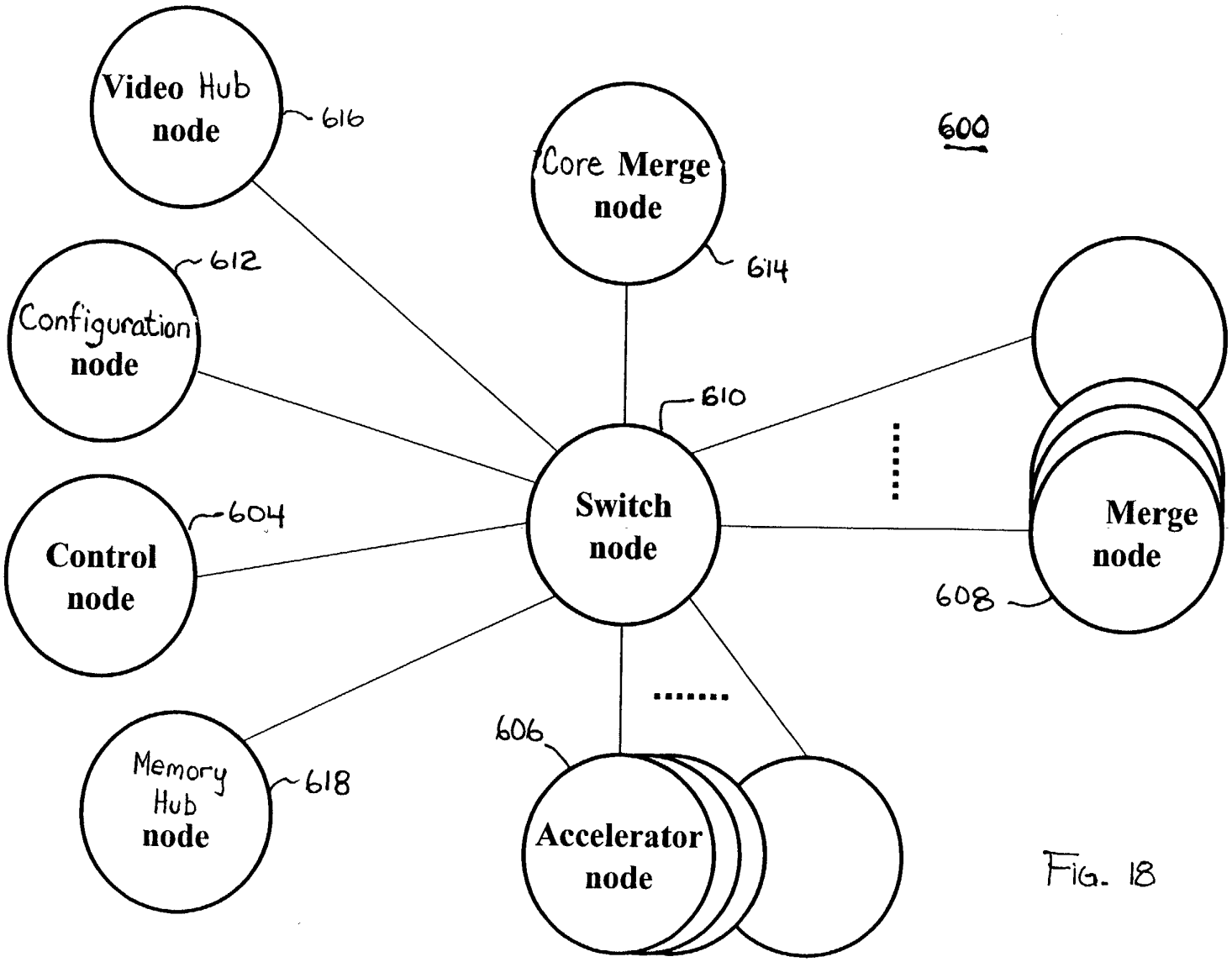

Fig. 18

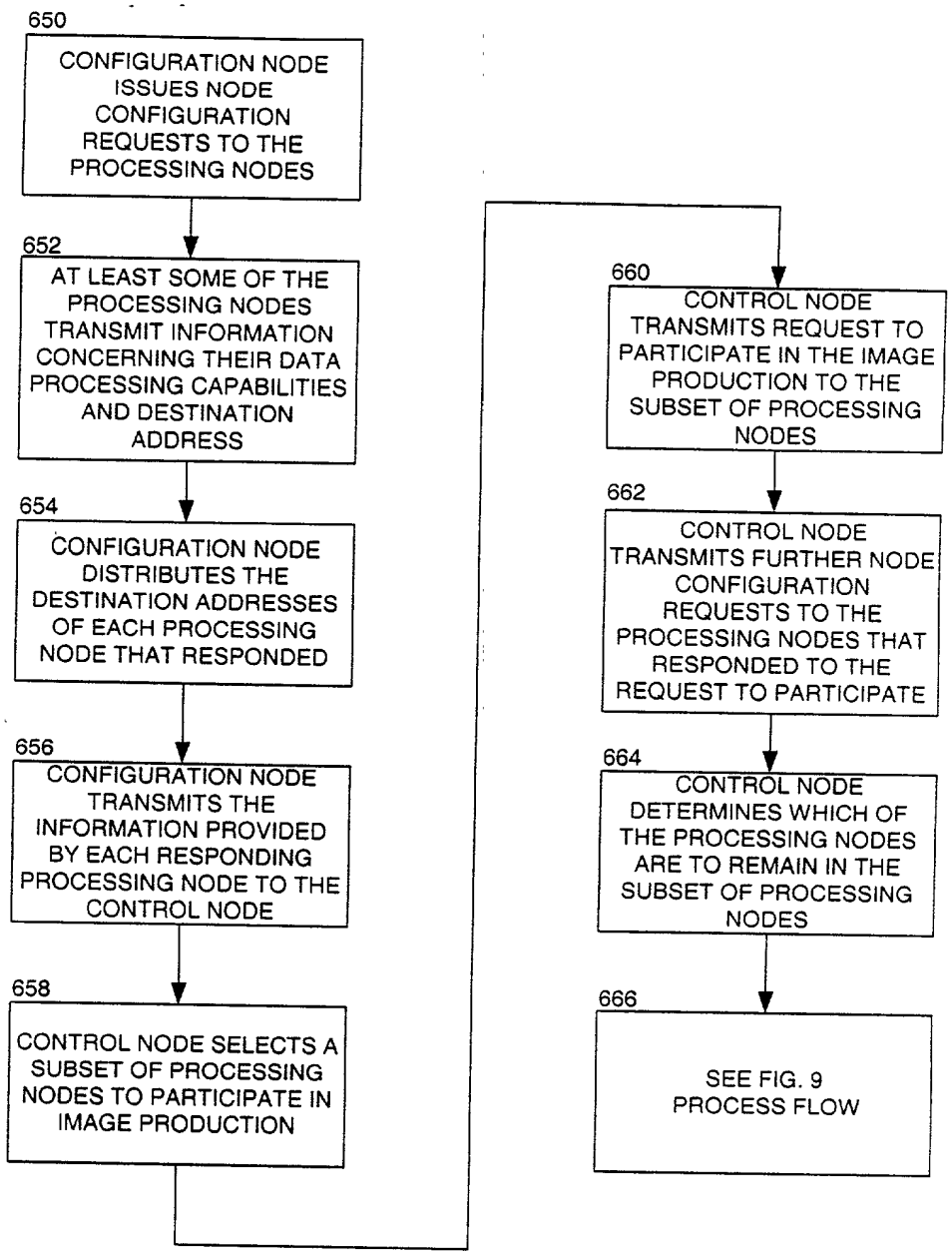
650
CONFIGURATION NODE ISSUES NODE CONFIGURATION REQUESTS TO THE PROCESSING NODES
652
AT LEAST SOME OF THE PROCESSING NODES TRANSMIT INFORMATION CONCERNING THEIR DATA PROCESSING CAPABILITIES AND DESTINATION ADDRESS
654
CONFIGURATION NODE DISTRIBUTES THE DESTINATION ADDRESSES OF EACH PROCESSING NODE THAT RESPONDED
656
CONFIGURATION NODE TRANSMITS THE INFORMATION PROVIDED BY EACH RESPONDING PROCESSING NODE TO THE CONTROL NODE
658
CONTROL NODE SELECTS A SUBSET OF PROCESSING NODES TO PARTICIPATE IN IMAGE PRODUCTION
660
CONTROL NODE TRANSMITS REQUEST TO PARTICIPATE IN THE IMAGE PRODUCTION TO THE SUBSET OF PROCESSING NODES
662
CONTROL NODE TRANSMITS FURTHER NODE CONFIGURATION REQUESTS TO THE PROCESSING NODES THAT RESPONDED TO THE REQUEST TO PARTICIPATE
664
CONTROL NODE DETERMINES WHICH OF THE PROCESSING NODES ARE TO REMAIN IN THE SUBSET OF PROCESSING NODES
666
SEE FIG. 9 PROCESS FLOW

FIG. 19

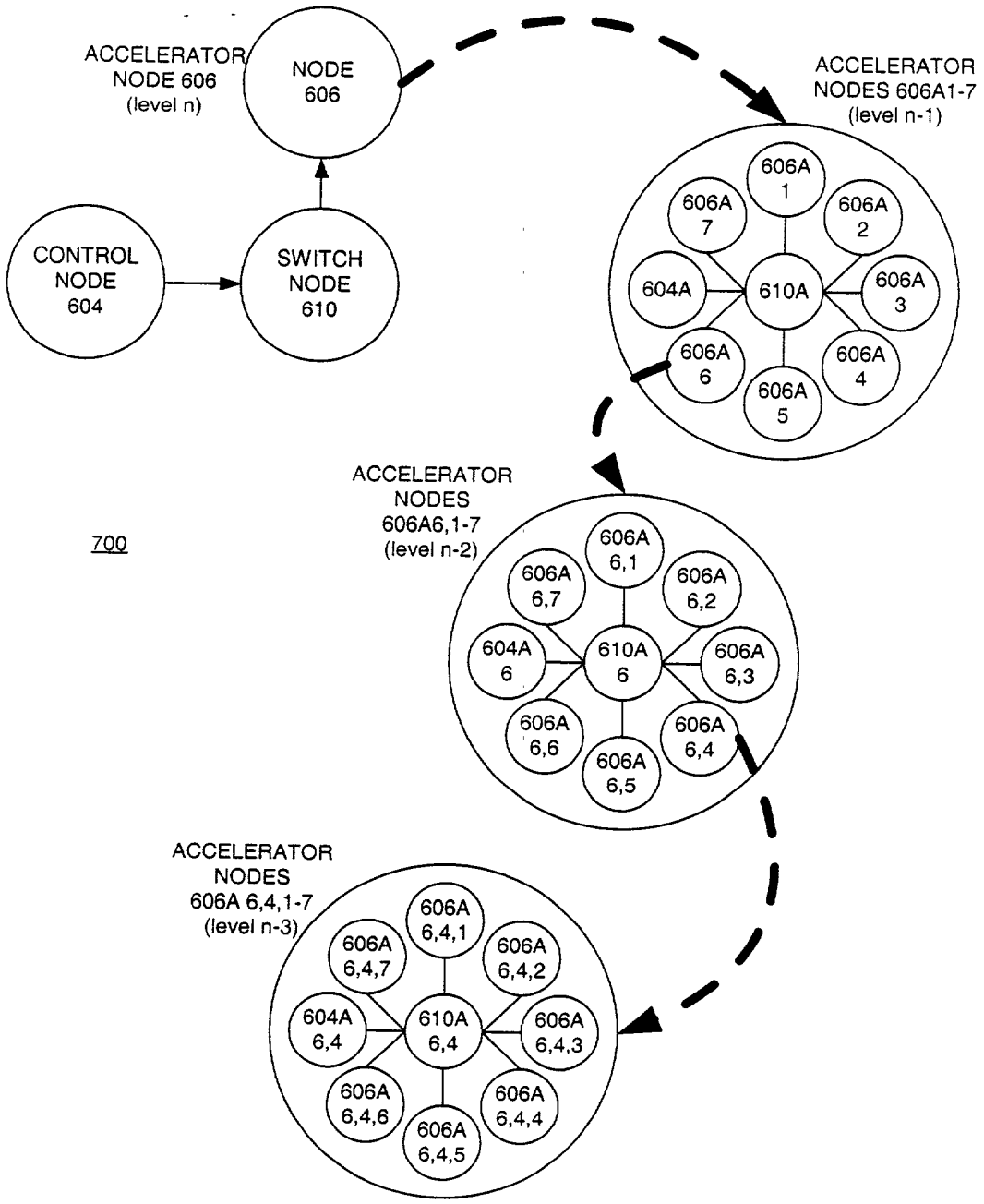
ACCELERATOR NODE 606 (level n)
NODE 606
CONTROL NODE 604
SWITCH NODE 610
ACCELERATOR NODES 606A1-7 (level n-1)
606A 1
606A 2
606A 3
606A 4
606A 5
606A 6
606A 7
604A
610A
700
ACCELERATOR NODES 606A6,1-7 (level n-2)
606A 6,1
606A 6,2
606A 6,3
606A 6,4
606A 6,5
606A 6,6
606A 6,7
604A 6
610A 6
ACCELERATOR NODES 606A 6,4,1-7 (level n-3)
606A 6,4,1
606A 6,4,2
606A 6,4,3
606A 6,4,4
606A 6,4,5
606A 6,4,6
606A 6,4,7
604A 6,4
610A 6,4

FIG. 20

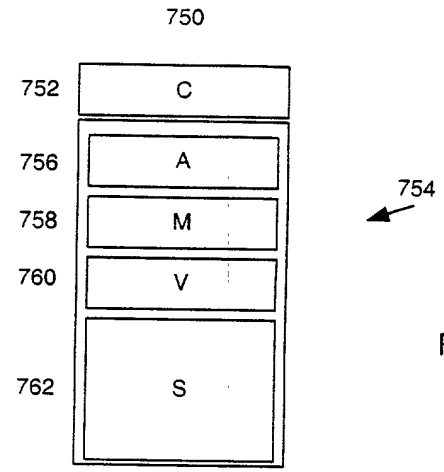

FIG. 21A

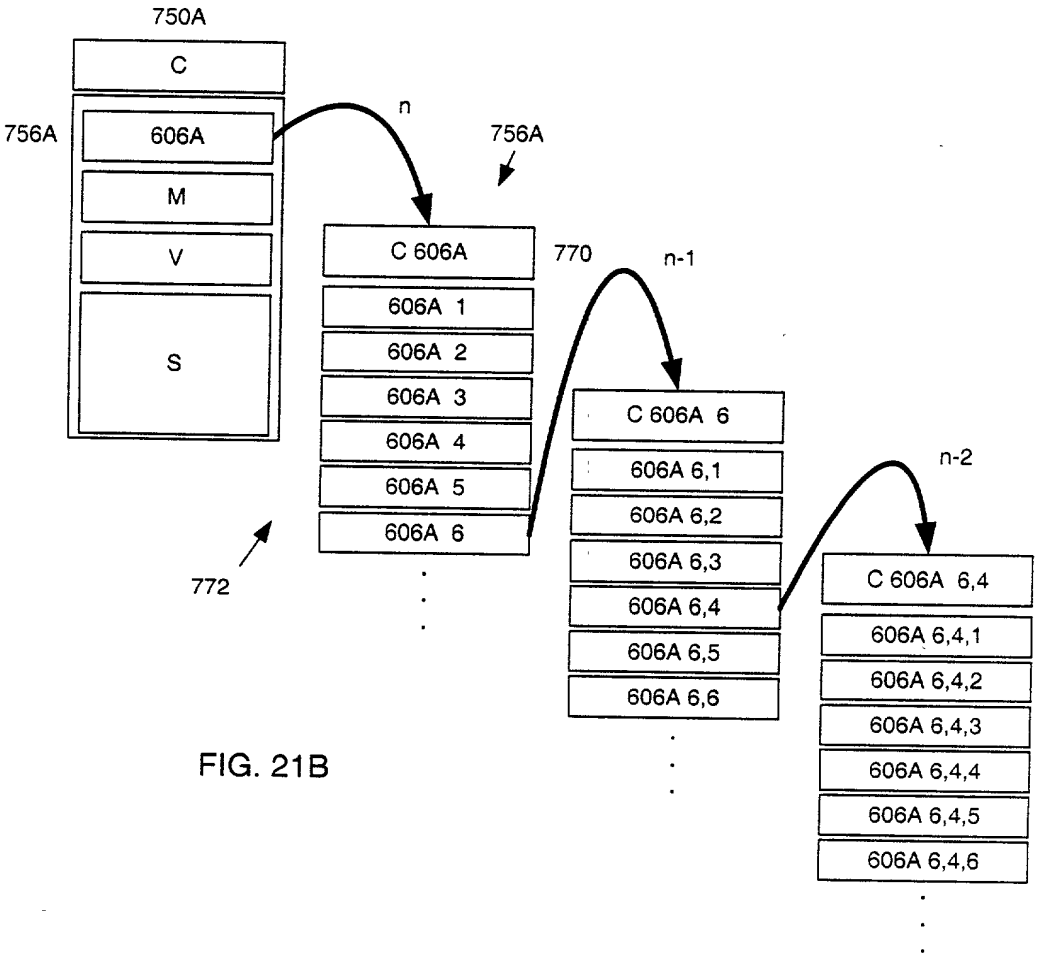

FIG. 21B